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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,761	06/18/2001	Andrew Popplewell	00-387 1496.00089	2432

24319 7590 06/02/2004

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,761	POPPLEWELL ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 8* is/are rejected.

7)☒ Claim(s) *2-7 and 9-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/28/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in United Kingdom on October 31, 2000. It is noted, however, that applicant has not filed a certified copy of the GB 00 26614.8 application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

The information disclosure statement (IDS) submitted on September 28, 2001 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

Figure 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to because Figures 3 and 4 have a graph with the axis not defined. Descriptive labels other than numerical are needed for figures 3-4. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required

in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al. U.S. Patent No. 4,234,954 in view of Mock U.S. Patent No. 5,828,678.

As per claims 1 and 8, Lange et al. teach a system and method of error estimation in which the clock pulses are at the same rate as the data rate operating on the theory that a circuit can be devised which counts, the rate at which the combined signal plus noise voltage exceeds REF+2 V (where REF is the mean voltage around which the input signal is biased, V is the average maximum voltage above REF for a binary 1, and -V is the average minimum voltage below REF for a binary 0), and the rate at which the combined signal plus noise is less than REF-2 V. The sum of these two rates ("positive errors" plus "negative errors") provides a good approximation of the BER on the input data stream because these two events are mutually exclusive (column 2 lines 20-46, column 5 lines 34-42, claim 9, Figure 20). Not explicitly disclosed is the multiple clocks and the ratio calculation.

However, in an analogous art, Mock teaches a system and method in which a resolving system provides an output clock signal having an output clock frequency that is a predetermined rational multiple of an input clock frequency of an input signal to the resolving system. The resolving system includes a first counter that counts clock pulses of the input clock signal to provide a first value, a second counter that counts clock pulses of the output clock signal to provide a second value, a processor that computes a difference between a ratio of the first and second values with the predetermined

rational multiple and generates an error signal based on the difference, and a direct digital synthesis unit that receives the error signal, and based on the error signal generates the output clock signal (column 4 lines 4-62, claim 17). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the multiple clock signals of Mock with the error estimation system of Lange et al. This would have been obvious as suggested by Mock in order to provide higher quality output signals for a variety of input signals (column 3 lines 51-61).

Allowable Subject Matter

Claims 2-7 and 9-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 6,577,690 Barman et al.

This patent teaches a method and apparatus that computes an optimal estimate of known clock frequency error between the transmitter and receiver using a known pilot signal and the statistics of the noise process. The estimate is computed such that the

residual clock error is below the least count (the smallest frequency correction that can be imparted) of the VCXO that controls the receiver sample clock. A tracking technique based on a measure of drift in taps of frequency domain equalizers of different sub-carriers is disclosed. This tracking ensures that the residual mean square error is within a predefined bound. Finally, the least count effects in digitally controlled oscillators (DAC controlled VCXOs and Numerically Controlled Oscillators (NCXO)) are addressed by a dithering mechanism. The dithering mechanism involves imparting positive and negative clock corrections for different lengths of time in such a manner that the residual clock error becomes zero mean. In data mode, a tracking scheme makes uses of variations in frequency domain equalizer taps for determination of clock error estimates, computes a residual clock error estimate different from the clock error estimate generated from pilot channel using training mode scheme, and SNR based combination of errors is computed to obtain clock correction, and a dithering mechanism computes the actual correction to be given to the VCXO such that the residual phase error is maintained at an acceptably low value.

U. S. Patent No. 4,387,461 Evans

This patent teaches a data link conveying antipodal (two level) data bits, a signal quality measuring circuit using prestored experiential data acquired during a calibration phase. The circuit can measure any signal quality parameter, such as BER and SNR. The number of events falling within an error gate is compared with a more universal measure of bit events occurring during the sampling interval. These values are

translated into a quantitative measure of signal quality by means of a prestored lookup table. The error gates can be shaped to represent phase deviations, amplitude deviations, or any combination of phase and amplitude deviations. A wide dynamic range can be achieved by using several different gates of various shapes. The gates are derived from a bit synchronizer; the circuit functions without the necessity of superimposing upon the data streams any coding information.

"Estimation of the Percentile Maximum Time Interval Error of Gaussian White Phase Noise" Bregni et al. IEEE International Conference on Communications, Publication Date: 8-12 June 1997 On page(s): 1597 - 1601 vol.3 Inspec Accession Number: 5793974

This paper teaches that the MTIE is historically one of the main time-domain quantities considered for the specification of clock stability requirements in telecommunications standards. In this paper, MTIE is first introduced according to its classical definition and as a percentile quantity. Then, the percentile MTIE is estimated under the assumption of time error (TE) affected by Gaussian white phase modulation noise, by deriving the probability distribution, of the TE spanned range as a function of the noise standard deviation σ. The formulas derived here may allow interpretation of common Allan-variance factory specifications in terms of percentile MTIE as well. In order to support the theory with sound experimental evidence, some results measured on state-of-the-art telecommunications clocks are provided.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

Cynthia Britt
Examiner
Art Unit 2133

Guy J. Lamarre
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